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[Using IPC Variation in Workloads with Externally.. - Ghiasi, Casmira.. \(2000\) \(Correct\) \(15 citations\)](#)  
 tasks)We have implemented an architectural **simulator** that uses an **IPC** specification to indicate the  
 Using **IPC** Variation in Workloads with Externally Specified  
[cse1.cs.colorado.edu/~ghiasi/papers/ipcm/ipcm-wced-2k.ps](http://cse1.cs.colorado.edu/~ghiasi/papers/ipcm/ipcm-wced-2k.ps)

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[Optimization of Instruction Fetch Mechanisms for High.. - Conte, Menezes, Mills.. \(1995\) \(Correct\) \(71 citations\)](#)  
 cache misses are not explicitly modeled in the **simulator**. The PI4 model has two fixed-point units  
 comparisons are based on simulated results of the **IPC** for three microarchitectures. The results show  
[www4.ncsu.edu/eos/users/c/conte/www/isca95c.ps](http://www4.ncsu.edu/eos/users/c/conte/www/isca95c.ps)

[The Impact of Operating System Structure on Memory System.. - Chen, Bershad \(1993\) \(Correct\) \(85 citations\)](#)  
 (**IPC**)threads, and virtual memory. HigherThe **simulator** consumes user and system traces while they  
 using the parameters shown in Table 2-1. munication (**IPC**)threads, and virtual memory. HigherThe **simulator**  
[guir.cs.berkeley.edu/projects/osprelims/papers/impact-os-mem.ps.gz](http://guir.cs.berkeley.edu/projects/osprelims/papers/impact-os-mem.ps.gz)

[An Analysis of Database Workload Performance on.. - Lo, Barroso.. \(1998\) \(Correct\) \(28 citations\)](#)  
 workloads to drive a highlydetailed trace-driven **simulator** for an 8-context, 8-wide simultaneous  
 a transaction processing workload achieves only 0.79 **IPC** on an 8wide, out-of-order superscalar with 128KB  
[ftp.digital.com/pub/Digital/WRL/research-reports/WRL-TR-98.10.ps.gz](http://ftp.digital.com/pub/Digital/WRL/research-reports/WRL-TR-98.10.ps.gz)

[An Adaptive Issue Queue for Reduced Power at High.. - Alper Buyuktosunoglu.. \(2000\) \(Correct\) \(8 citations\)](#)  
 the authors use a trace-driven power-performance **simulator** (based on the model by Cai [7])to report  
 or the power [4] without significantly impacting the **IPC** performance. In [3]the authors propose and  
[www.ee.princeton.edu/~dbrooks/pacs2000\\_2.ps](http://www.ee.princeton.edu/~dbrooks/pacs2000_2.ps)

[Efficacy and Performance Impact of Value Prediction - Rychlik, Faistl, Krug, Shen \(1998\) \(Correct\) \(20 citations\)](#)  
 are generated by an execution-driven performance **simulator** [2]The **simulator** uses a cycle-accurate  
 This design is able to achieve 8.6% to 20% **IPC** improvements on the SPEC benchmarks. Additionally,  
[www.ece.cmu.edu/~cmuart/techreport/bohoslav/CMuART-1998-04.ps](http://www.ece.cmu.edu/~cmuart/techreport/bohoslav/CMuART-1998-04.ps)

[Efficient Incremental Run-Time Specialization for Free - Marlet, Consel, Boinot \(1999\) \(Correct\) \(10 citations\)](#)  
 For example, a generic microprocessor **simulator** can be first specialized with respect to a  
 was used by Volansch to optimize the Chorus **IPC** [34]1.4 This paper In this paper, we study how  
[www.irisa.fr/compose/papers/incrpe.ps.gz](http://www.irisa.fr/compose/papers/incrpe.ps.gz)

[An Analysis of Operating System Behavior on a.. - Redstone, Eggers, Levy \(2000\) \(Correct\) \(6 citations\)](#)  
 and (2) integrated our SMT Alpha instruction set **simulator** into the SimOS **simulator** to provide an  
 the workload? In particular, we wish to verify the **IPC** results of previous studies to see whether they  
[www.cs.washington.edu/research/smt/papers/os.ps](http://www.cs.washington.edu/research/smt/papers/os.ps)

[Branch Classification: a New Mechanism for Improving Branch.. - Chang \(1994\) \(Correct\) \(34 citations\)](#)  
 of these functions calls the branch predictor **simulator** to generate the branch prediction and to update  
 the branch penalty is defined as  $C * (1-p) * r * \text{ipc}$  where C denotes the number of cycles wasted due  
[www.eecs.umich.edu/HPS/pub/class\\_micro27.ps](http://www.eecs.umich.edu/HPS/pub/class_micro27.ps)

Evaluating Non-deterministic Multi-threaded.. - Alameldeen, Mauer.. (2002) (Correct) (2 citations)  
development of commercial workloads for timing **simulators**. We describe how we address these challenges in

counters and calculated the Instruction Per Cycle (IPC) and cache miss rates as observed on the real  
[tesla.hpl.hp.com/caecw-02/s2p1.pdf](http://tesla.hpl.hp.com/caecw-02/s2p1.pdf)

Tornado: maximizing locality and concurrency in a shared-memory.. - Gamsa (1999) (Correct) (8 citations)  
and use on both NUMA machine and a complete machine **simulator**, SimOS. ii A N D O T O R Preface Like most design, the process management design, and the IPC design. I was also responsible for most of the In addition, Tornado includes a new **interprocess communication** facility, called the Protected  
[www.eecg.toronto.edu/~ben/thesis.ps.gz](http://www.eecg.toronto.edu/~ben/thesis.ps.gz)

Tornado: Maximizing Locality and Concurrency in a.. - Gamsa, Krieger.. (1999) (Correct) (8 citations)  
on Toronto's NUMA hardware and on the SimOS **simulator**. 1 Introduction Traditional multiprocessor that preserves the locality and concurrency of IPC's, and (iii) a new locking strategy that allows has been handed to the cleanup system. 6 **Interprocess communication** In a microkernel system like Tornado  
[www.research.ibm.com/K42/osdi-preprint.ps](http://www.research.ibm.com/K42/osdi-preprint.ps)

Dynamically Reconfiguring Processor Resources to Reduce Power .. - Roberto Maro Yu (2000) (Correct) (5 citations)  
disabled. 2 Experimental Methodology The **simulator** used in this study is derived from the SIM-2.5 3.5 x 10 0.5 1.5 2.5 3.5 Figure 1: Variation in IPC over time for the hydro2d benchmark. Previous  
[ftp.lems.brown.edu/cad/irispapers/pacs00.ps.gz](http://ftp.lems.brown.edu/cad/irispapers/pacs00.ps.gz)

Adaptive Thermal Management for High-Performance Microprocessors - Brooks, Martonosi (2000) (Correct) (5 citations)  
that last on the or- Cycle-Level Performance **Simulator** Parameterizable Power Models Cycle-by-Cycle techniques by investigating the correlation between IPC, power dissipation, and various architectural  
[www.ee.princeton.edu/~dbrooks/complex2000.ps](http://www.ee.princeton.edu/~dbrooks/complex2000.ps)

Time Varying Behavior of Programs - Timothy Sherwood Brad (1999) (Correct) (7 citations)  
for this study. Section 3 describes the **simulator** and architecture model used. Section 4 course of execution correlating the behavior between IPC, branch prediction, value prediction, address  
[www.cse.ucsd.edu/~calder/papers/UCSD-CS99-630.pdf](http://www.cse.ucsd.edu/~calder/papers/UCSD-CS99-630.pdf)

The Non-Critical Buffer: Using Load Latency Tolerance to.. - Fisk, Bahar (1999) (Correct) (7 citations)  
main cache. In this study we use a cycle-level **simulator** of an 8-issue, speculative, out-of-order than other traditional cache improvement schemes. IPC improvements of over 4% are seen for some  
[ftp.lems.brown.edu/cad/irispapers/iccd99.ps.gz](http://ftp.lems.brown.edu/cad/irispapers/iccd99.ps.gz)

A Circuit Level Implementation of an Adaptive.. - Buyuktosunoglu.. (2001) (Correct) (2 citations)  
the authors use a trace-driven power-performance **simulator** (based on the model by Cai [5] to report or the power [8] without significantly impacting the IPC (instruction per cycle) performance. In [6] the  
[www.ece.rochester.edu/~albonesi/research/papers/glsvisi01.ps](http://www.ece.rochester.edu/~albonesi/research/papers/glsvisi01.ps)

Confidence Estimation for Branch Prediction Reversal - Aragón, González, García.. (2001) (Correct) (2 citations)  
using a modified version of the sim-safe **simulator** [2] The number of branch hits and misses of a rate, as well as its performance in terms of IPC. Finally, Section 5 summarizes the conclusions of  
[www.ditec.um.es/~jlaragon/papers/BPRU-HIPC-2001.pdf](http://www.ditec.um.es/~jlaragon/papers/BPRU-HIPC-2001.pdf)

Predictive Techniques for Aggressive Load Speculation - Glenn Reinman (1998) (Correct) (10 citations)  
8. 2 Methodology and Baseline Architecture The **simulators** used in this study are derived from the Base %ld %st Program Input exec (M) fastfwd (M) IPC exe exe compress ref 93 0 1.93 26.7 9.5 gcc  
[www-cse.ucsd.edu/users/calder/papers/MICRO-98-LoadSpec.ps](http://www-cse.ucsd.edu/users/calder/papers/MICRO-98-LoadSpec.ps)

Streamlining Data Cache Access with Fast Address Calculation - Austin, Pnevmatikatos, Sohi (1995) (Correct) (19 citations)  
4-way in-order issue superscalar processor **simulator** with a 16k directmapped non-blocking data

Per Cycle Figure 2: Impact of Load Latency on **IPC**. calculation. If the address is mispredicted, the  
ftp.cs.wisc.edu/sohi/papers/1995/isca.fast.ps.gz

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